REMARKS/ARGUMENTS

The Examiner is thanked for the courteous telephone interview granted Applicants' representative on August 8, 2006. This Response has been prepared pursuant to comments and suggestions made during the interview.

Amendments were made to the specification to supply serial number and filing date information regarding applications referred to in the specification. No new matter has been added by any of the amendments to the specification.

Claims 1-26 are pending in the present application. Claims 1, 3, 12, 14 and 23 were amended. No claims have been added and no claims have been canceled. Support for the amendments to claims 1, 12 and 23 can be found, for example, on page 49, lines 24-27. Applicants believe claims 1-26 patentably distinguish over the cited art in their present form, and respectfully request reconsideration of the rejection in view of the above amendments and the following comments.

I. 35 U.S.C. § 112, Second Paragraph

The Examiner has rejected claims 3, 4, 12, 14, 15, and 24 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter, which Applicants regard as the invention. This rejection is respectfully traversed.

By the present Amendment, claims 3, 12 and 14 have been amended to correct the informalities noted by the Examiner, and are now believed to fully satisfy the requirements of 35 U.S.C. § 112, second paragraph. The Examiner is thanked for bringing these matters to Applicants' attention.

With respect to the rejection of claims 4, 15 and 24, however, Applicants believe the claims include proper antecedent proper antecedent basis for the term "the subsequent memory location" recited therein. During the above-referenced interview the Examiner acknowledged that these claims appeared to satisfy the requirements of 35 U.S.C. § 112, second paragraph, in their present form, and that the rejection of those claims under 35 U.S.C. § 112, second paragraph, would be withdrawn.

Therefore, the rejection if claims 3, 4, 12, 14, 15, and 24 under 35 U.S.C. § 112, second paragraph, has been overcome.

II. 35 U.S.C. § 101

The Examiner has rejected claims 23-26 under 35 U.S.C. § 101 as being directed towards non-statutory subject matter. This rejection is respectfully traversed.

The Examiner contends that a computer readable medium which includes radio frequency waves and wireless communication links as defined in the specification, constitutes non-statutory subject matter. Applicants respectfully disagree.

Applicants submit that no basis is present for holding a computer readable medium claim non-statutory because the medium may be allegedly "intangible." The MPEP states:

> In this context, "functional descriptive material" consists of **data structures** and computer programs **which impart functionality when employed as a computer componen**t. (The definition of "data structure" is "a physical or logical relationship among data elements, designed to support specific data manipulation functions." The New IEEE Standard Dictionary of Electrical and Electronics Terms 308 (5th ed. 1993).) "Nonfunctional descriptive material" includes but is not limited to music, literary works and a compilation or mere arrangement of data.
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> **When functional descriptive material is recorded on some computer-readable medium it becomes structurally and functionally interrelated to the medium and will be statutory in most cases since use of technology permits the function of the descriptive material to be realized.** Compare *In re Lowry*, 32 F.3d 1579, 1583-84, 32 USPQ2d 1031, 1035 (Fed. Cir. 1994) (claim to data structure stored on a computer readable medium that increases computer efficiency held statutory) and *Warmerdam*, 33 F.3d at 1360-61, 31 USPQ2d at 1759 (claim to computer having a specific data structure stored in memory held statutory product-by-process claim) with *Warmerdam*, 33 F.3d at 1361, 31 USPQ2d at 1760 (claim to a data structure *per se* held nonstatutory). **(emphasis added)**

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Claims 23-26 clearly recite functional descriptive material since they impart functionality when employed as a computer component. Moreover, the functional descriptive material of claims 23-26 is recorded on "some" computer-readable medium.

In the above context, the term "some" means "any" computer-readable medium. The MPEP does not draw any distinctions between one type of media that is considered to be statutory and another type of media that is considered to be non-statutory. To the contrary, the MPEP clearly states that as long as the functional descriptive material is in "some" computer-readable medium, it should be considered statutory. The only exceptions to this statement in the MPEP are functional descriptive material that does not generate a useful, concrete and tangible result, e.g., functional descriptive material composed completely of pure mathematical concepts that provide no practical result. Claims 23-26 clearly recite a useful, concrete and tangible result in that coverage data for accesses to dynamically allocated data is generated for use during execution of code. This is not just some disembodied mathematical concept or abstract idea.

Thus, claims 23-26 are directed to functional descriptive material that provides a useful, concrete and tangible result, and which is embodied on "some" computer-readable medium. Therefore, claims 23-26 are statutory and the rejection of the claims under 35 U.S.C. § 101 has been overcome.

III. 35 U.S.C. § 102, Anticipation

The Examiner has rejected claims 1-8, 10-19, and 21-26 under 35 U.S.C. § 102(b) as being anticipated by Hervin et al. (U.S. Patent No. 5,805,879). This rejection is respectfully traversed.

As to claim 1, the Office Action states:

a. **As for Claim 1**, FROG discloses a method in a data processing system for generating coverage data for accesses to dynamically allocated data during execution of code in a data processing system **[Column 1, Lines 16-22]**, the method comprising: responsive to a request to dynamically allocate a memory area for dynamically allocated data, dynamically allocating the memory area **[Column 3, Lines 53-56]**; responsive to dynamically allocating the memory area, associating the memory area with a data access indicator **[Column 3, Line 66 – Column 4, Line 10]**; responsive to executing an instruction in the code at a processor in the data processing system, determining whether an access to a memory location associated with the data access indicator has occurred **[Figure 7, #715 & Column 4, Lines 24-44]**; and if the data access indicator is associated with the memory area, changing a state of the data access indicator by the processor when the instruction is executed **[Figure 7, #730]**, wherein the coverage data for the dynamically allocated data is generated during execution of the code by the processor **[Column 11, Line 55 – Column 12, Line 11]**.

Office Action dated May 15, 2006, pages 4-5.

Claim 1 as amended herein is as follows:

1. A method in a data processing system for generating coverage data for accesses to dynamically allocated data during execution of code in a data processing system, the method comprising:

responsive to a request to dynamically allocate a memory area for dynamically allocated data during runtime when an allocation of memory is required, dynamically allocating the memory area;

responsive to dynamically allocating the memory area, associating the memory area with a data access indicator;

responsive to executing an instruction in the code at a processor in the data processing system, determining whether an access to a memory location associated with the data access indicator has occurred; and

if the data access indicator is associated with the memory area, changing a state of the data access indicator by the processor when the instruction is executed, wherein the coverage data for the dynamically allocated data is generated during execution of the code by the processor.

A prior art reference anticipates a claimed invention under 35 U.S.C. § 102 only if every element of the claimed invention is identically shown in that single prior art reference, arranged as they are in the claims. *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). All limitations of a claimed invention must be considered when determining patentability. *In re Lowry*, 32 F.3d 1579, 1582, 32 U.S.P.Q.2d 1031, 1034 (Fed. Cir. 1994). Anticipation focuses on whether a claim reads on the product

or process a prior art reference discloses, not on what the reference broadly teaches. *Kalman v. Kimberly-Clark Corp.*, 713 F.2d 760, 218 U.S.P.Q. 781 (Fed. Cir. 1983).

Applicants respectfully submit that Hervin et al. (hereinafter "Hervin") does not identically show every element of the claimed invention arranged as they are in the claims; and, accordingly, does not anticipate the claims. With respect to claim 1, in particular, Hervin does not teach or suggest "responsive to a request to dynamically allocate a memory area for dynamically allocated data during runtime when an allocation of memory is required, dynamically allocating the memory area", or "responsive to dynamically allocating the memory area, associating the memory area with a data access indicator".

In rejecting the claims, the Examiner refers to column 3, lines 53-56 and column 3, line 66 to column 4, line 10 of Hervin as disclosing these features. Column 3, line 53 to Col. 4, line 10 of Hervin is as follows:

> To address the above-discussed deficiencies of the prior art, it is a primary object of the present invention to provide a way to mark segments of memory as having been accessed.
>
> In the attainment of the above primary object, the present invention provides, in a pipelined processor having at least one execution pipeline for executing instructions, the execution pipeline including ID (decode), AC (address calculation), and EX (execution) processing stages, the processor capable of addressing segments of system memory coupled thereto, a circuit for, and method of setting a segment access indicator associated with a segment of the system memory being accessed by the processor.
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> The circuit includes: (a) exception generating circuitry to generate an exception when the segment access indicator requires setting and (b) exception handling circuitry, invoked by the processor in response to generation of the exception, to flush the execution pipeline of instructions following a segment load instruction, set the segment access indicator and load an address pointer of the processor with an address corresponding to a specified location within the segment. The "specified location within the segment" maybe the instruction following the segment load instruction or may be another instruction, as appropriate. Regardless, the processor resumes execution of instructions.

The above recitation is generally directed to a mechanism for setting a segment access indicator associated with a segment of system memory as having been accessed by a processor. The recitation describes that exception generating circuitry generates an exception when a segment access indicator requires setting, and that the segment access indicator is set and an address pointer of a processor is loaded with an address corresponding to a specified location within the segment. The recitation does not, however, discuss how the memory segment is allocated or how the memory segment is associated with a segment access indicator, and clearly does not disclose that a memory area is dynamically allocated "responsive to a request to dynamically allocate a memory area for dynamically allocated data during runtime when an allocation of memory is required" as recited in claim 1. In addition, the reference also does not disclose "responsive to dynamically allocating the memory area, associating the memory area

with a data access indicator." Although Hervin may describe how an indicator may be set to indicate that a memory segment has been accessed, the reference does not disclose or suggest how a memory area is associated with a data access indicator, or that a memory area is dynamically allocated "responsive to a request to dynamically allocate a memory area for dynamically allocated data during runtime when an allocation of memory is required".

During the interview, the Examiner suggested that it could be implied that Hervin operated dynamically, and referred in particular, to the recitation bridging columns 11 and 12 of Hervin. This recitation, however, relates to setting the segment access indicator when the processor accesses a segment in memory. It does not describe dynamically allocating a memory area during runtime when an allocation of memory is required, nor does it discuss associating the memory area with a data access indicator responsive to dynamically allocating the memory area.

For at least all the above reasons, Claim 1 is not anticipated by Hervin and patentably distinguishes over Hervin in its present form.

Claims 2-8, 10 and 11 depend from and further restrict claim 1, and are also not anticipated by Hervin, at least by virtue of their dependency. Many of these claims, however, recite additional features that are not disclosed or suggested by Hervin. For example, claim 3 recites that "the data access indicator includes an identification of one byte beyond the ending location and wherein an access to the one byte beyond the ending location indicates that a memory size of the memory area is insufficient". In rejecting this claim, the Examiner refers to Col. 4 lines 4-10 reproduced above. The recitation, however, does not disclose that a data access indicator includes "an identification of one byte beyond the ending location and wherein an access to the one byte beyond the ending location indicates that a memory size of the memory area is insufficient", nor is such a teaching inherent or otherwise suggested in the recitation. Claim 3, accordingly, patentably distinguishes over Hervin in its own right as well as by virtue of its dependency.

Independent claims 12 and 23 have been amended in a manner similar to claim 1 and recite similar subject matter as claim 1. These claims are also not anticipated by Hervin for similar reasons as discussed above with respect to claim 1. Claims 13-19, 21-22 and 24-26 depend from and further restrict one of claims 12 and 23, and are also not anticipated by Hervin.

Therefore, the rejection of claims 1-8, 10-19, and 21-26 under 35 U.S.C. § 102 has been overcome.

IV. 35 U.S.C. § 103, Obviousness

The Examiner has rejected claims 9 and 20 under 35 U.S.C. § 103(a) as being unpatentable over Hervin et al. (U.S. Patent No. 5,805,879) as applied to claims 1 and 12 above, and further in view of Sederlund et al. (U.S. Patent No. 6,647,301 B1). This rejection is respectfully traversed.

Claims 9 and 20 depend from and further restrict claims 1 and 12, respectively. Sederalund is cited as disclosing an access indicator associated with an instruction located in a shadow memory. Sederlund does not, however, supply the deficiencies in Hervin as described above, and claims 9 and 20 patentably distinguish over the references in their present form.

Therefore, the rejection of claims 9 and 20 under 35 U.S.C. § 103 has been overcome.

V. Conclusion

For all the above reasons, it is respectfully urged that claims 1-26 are allowable in their present form, and that this application is now in condition for allowance. It is, accordingly, respectfully requested that the Examiner so find and issue a Notice of Allowance in due course.

The Examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the Examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

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Respectfully submitted,

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